Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated programmable digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC); and

a digital calibration circuit including a memory for storing predetermined end point coefficients of said digital to analog converter transfer function, said end point coefficients including a zero scale and a full scale coefficient; and an arithmetic logic unit for applying the end point coefficients to the DAC input signal to adjust the end points of said DAC.

2-6. (cancelled)

7. (currently amended) The integrated programmable digital calibration circuit and digital to analog converter of claim ~~6~~ 1 in which said arithmetic logic unit includes an arithmetic circuit for algebraically counting the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale coefficient and applying those coefficients to the input signal to the DAC.

8. (original) The integrated programmable digital calibration circuit and digital to analog converter of claim 1 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

9. (original) The integrated programmable digital calibration circuit and digital to analog converter of claim 8 in which said memory is in said digital calibration circuit.

10. (original) The integrated programmable digital calibration circuit and digital to analog converter of claim 8 in which said memory is external to said digital calibration circuit.

11. (original) The integrated programmable digital calibration circuit and digital to analog converter of claim 8 in which said memory is a user accessible programmable memory.

12. (currently amended) A programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

an analog signal circuit responsive to said DAC; and

a digital calibration circuit including a memory for storing the predetermined end point coefficients of said DAC transfer function, said end point coefficients including a zero scale and a full scale coefficient; and an arithmetic logic unit for applying the end point coefficients to the DAC input signal to adjust for the end points of said DAC and said analog signal circuit.

13. (original) The programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter of claim 12 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

14. (original) The programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter of claim 13 in which said memory is in said digital calibration circuit.

15. (original) The programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter of claim 13 in which said memory is external to the digital calibration circuit.

16. (original) The programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter of claim 13 in which said memory is a user accessible programmable memory.

17. (currently amended) A programmable integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter; and

a digital calibration circuit including a memory for storing the predetermined offset coefficient and gain coefficient of said digital to analog converter (DAC) and an arithmetic logic unit including an arithmetic circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient and an adder circuit for adding the

offset coefficient to said input signal to adjust the gain and offset of said DAC, said arithmetic circuit including a divider circuit for dividing the product of the DAC input and the gain coefficient before adding it to the offset coefficient.

18-19. (cancelled)

20. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 17 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

21. (currently amended) The programmable integrated digital calibration circuit and digital to analog converter of claim ~~18~~ 17 in which said memory is in said digital calibration circuit.

22. (currently amended) The programmable integrated digital calibration circuit and digital to analog converter of claim ~~18~~ 17 in which said memory is external to said digital calibration circuit.

23. (currently amended) The programmable integrated digital calibration circuit and digital to analog converter of claim ~~18~~ 17 in which said memory is a user accessible programmable memory

24. (currently amended) A programmable digital calibration system including ~~a~~ an integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

an analog signal circuit responsive to said DAC; and

a digital calibration circuit including a memory for storing the predetermined offset coefficient and gain coefficient of said DAC and said analog signal circuit; and an arithmetic logic unit including an arithmetic circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient and an adder circuit for adding the offset coefficient to said input signal to adjust the gain and offset of said DAC and said analog signal circuit, said arithmetic circuit including a divider circuit for dividing the product of the DAC input and the gain coefficient before adding it to the offset coefficient.

25-26. (cancelled)

27. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 24 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

28. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 24 in which said memory is in said digital calibration circuit.

29. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 24 in which said memory is external to said digital calibration circuit.

30. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 24 in which said memory is a user accessible programmable memory.

31. (original) A programmable integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC); and

a digital calibration circuit including a memory for storing predetermined zero scale and full scale coefficients of said digital to analog converter (DAC) and an arithmetic logic unit including an arithmetic circuit for algebraically combining the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale coefficient and applying those coefficients to the input signal to the DAC to adjust the zero scale and full scale of said DAC.

32. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 31 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

33. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 32 in which said memory is in said digital calibration circuit.

34. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 32 in which said memory is external to said digital calibration circuit.

35. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 32 in which said memory is a user accessible programmable memory.

36. (original) A programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

an analog or mixed signal circuit responsive to said DAC; and

a digital calibration circuit including a memory for storing predetermined zero scale and full scale coefficients of said DAC and said analog signal circuit; and an arithmetic logic unit including an arithmetic circuit for algebraically combining the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale coefficient and applying those coefficients to the input signal of the DAC to adjust for the zero scale and full scale offsets of said DAC and said analog signal circuit.

37. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 36 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

38. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 37 in which said memory is in said digital calibration circuit.

39. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 37 in which said memory is external to said digital calibration circuit.

40. (original) The programmable integrated digital calibration circuit and digital to analog converter of claim 37 in which said memory is a user accessible programmable memory.

41. (currently amended) An integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC); and

a digital calibration circuit including a memory for storing predetermined complements of the end point errors of said digital to analog converter transfer function, said complements of said end point errors including zero scale and full scale error coefficients; and an arithmetic logic unit for applying the complements of the end point errors to the DAC input signal to compensate for the end point errors of said DAC.

42-44. (cancelled)

45. (currently amended) The integrated digital calibration circuit and digital to analog converter of claim [[44]] 41 in which said arithmetic logic unit includes an arithmetic circuit for algebraically counting the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale error coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale error coefficient and applying those error coefficients to the input signal to the DAC.

46. (original) The integrated digital calibration circuit and digital to analog converter of claim 41 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

47. (original) The integrated digital calibration circuit and digital to analog converter of claim 46 in which said memory is in said digital calibration circuit.

48. (original) The integrated digital calibration circuit and digital to analog converter of claim 46 in which said memory is external to said digital calibration circuit.

49. (original) The integrated digital calibration circuit and digital to analog converter of claim 46 in which said memory is a user accessible programmable memory.

50. (currently amended) A digital calibration system including an integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

an analog signal circuit responsive to said DAC; and

a digital calibration circuit including a memory for storing the predetermined complements of the end point errors of said DAC transfer function, said complements of said end point errors including zero scale and full scale error coefficients; and an arithmetic logic unit for applying the complements of the end point errors to the DAC input signal to compensate for the end point errors of said DAC and said analog signal circuit.

51. (original) The digital calibration system integrated digital calibration circuit and digital to analog converter of claim 50 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

52. (original) The digital calibration system integrated digital calibration circuit and digital to analog converter of claim 51 in which said memory is in said digital calibration circuit.

53. (original) The digital calibration system integrated digital calibration circuit and digital to analog converter of claim 51 in which said memory is external to said digital calibration circuit.

54. (original) The digital calibration system integrated digital calibration circuit and digital to analog converter of claim 51 in which said memory is a user accessible programmable memory.

55-64. (cancelled)

65. (original) An integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC); and

a digital calibration circuit including a memory for storing predetermined zero scale and full scale error coefficients of said digital to analog converter (DAC) and an arithmetic logic unit including an arithmetic circuit for algebraically combining the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale error coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale error coefficient and applying those error coefficients to the input signal to the DAC to compensate for the zero scale and full scale errors of said DAC.

66. (original) The integrated digital calibration circuit and digital to analog converter of claim 65 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

67. (original) The integrated digital calibration circuit and digital to analog converter of claim 66 in which said memory is in said digital calibration circuit.

68. (original) The integrated digital calibration circuit and digital to analog converter of claim 66 in which said memory is external to said digital calibration circuit.

69. (original) The integrated digital calibration circuit and digital to analog converter of claim 66 in which said memory is a user accessible programmable memory.

70. (original) A digital calibration system including an integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

an analog or mixed signal circuit responsive to said DAC; and

a digital calibration circuit including a memory for storing predetermined zero scale and full scale error coefficients of said DAC and said analog signal circuit; and an arithmetic logic unit including an arithmetic circuit for algebraically combining the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale error coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale error coefficient and applying those error coefficients to the input signal of the DAC to compensate for the zero scale and full scale offset errors of said DAC and said analog signal circuit.

71. (original) The integrated digital calibration circuit and digital to analog converter of claim 70 in which said digital calibration circuit and DAC are on the same integrated circuit chip.

72. (original) The integrated digital calibration circuit and digital to analog converter of claim 71 in which said memory is in said digital calibration circuit.

73. (original) The integrated digital calibration circuit and digital to analog converter of claim 71 in which said memory is external to said digital calibration circuit.

74. (original) The integrated digital calibration circuit and digital to analog converter of claim 71 in which said memory is a user accessible programmable memory.

75. (new) An integrated programmable digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC); and

a digital calibration circuit including a memory for storing predetermined endpoint coefficients of said digital to analog converter transfer function; and an arithmetic logic unit for applying the end point coefficients to the DAC input signal to adjust the end points of said DAC, said end point coefficients including the offset coefficient and gain coefficient, said arithmetic logic unit including:

an arithmetic circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient,

an adder circuit for adding the offset coefficient to said input signal, and

a divider circuit for dividing the product of the DAC input and the gain coefficient before adding it to the offset coefficient.

76. (new) An integrated programmable digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC); and

a digital calibration circuit including a memory for storing predetermined endpoint coefficients of said digital to analog converter transfer function; and an arithmetic logic unit for applying the end point coefficients to the DAC input signal to adjust the end points of said DAC, said end point coefficients including the offset coefficient and gain coefficient, said arithmetic logic unit including:

an arithmetic circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient,

an adder circuit for adding the offset coefficient to said input signal, and

a second adder for combining a second constant with the gain coefficient before it is multiplied by the DAC input.

77. (new) An integrated programmable digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

a digital calibration circuit including a memory for storing predetermined end point coefficients of said digital to analog converter transfer function, said end point coefficients including a zero scale and a full scale coefficient; and

an arithmetic logic unit for applying the end point coefficients to the DAC input signal to adjust the end points of said DAC, said arithmetic logic unit including an arithmetic circuit for algebraically counting the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain the zero scale coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale coefficient and applying those coefficients to the input signal to the DAC.

78. (new) An integrated programmable digital calibration circuit and digital to analog converter comprising;

a digital to analog converter; and

a digital calibration circuit including a memory for storing the predetermined offset coefficient and gain coefficient of said digital to analog converter (DAC) and an arithmetic logic unit including an arithmetic circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient and an adder circuit for adding the offset coefficient to said input signal to adjust the gain and offset of said DAC, said arithmetic circuit including a second adder for combining a second constant with the gain coefficient before it is multiplied by the DAC input.

79. (new) A programmable digital calibration system including an integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC)

an analog signal circuit responsive to said DAC;

a digital calibration circuit including a memory for storing the predetermined offset coefficient and gain coefficient of said DAC and said analog signal circuit; and

an arithmetic logic unit including an arithmetic circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient and an adder circuit for adding the offset coefficient to said input signal to adjust the gain and offset of said DAC and said analog signal circuit, said arithmetic circuit including a second adder for combining a second constant with the gain coefficient before it is multiplied by the DAC input.

80. (new) An integrated digital calibration circuit and digital to analog converter comprising:

a digital to analog converter (DAC);

a digital calibration circuit including a memory for storing predetermined complements of the end point errors of said digital to analog converter transfer function, said complement of said end point errors including the zero scale and full scale error coefficients; and

an arithmetic logic unit for applying the complements of the end point errors to the DAC input signal to compensate for the end point errors of said DAC, said arithmetic logic unit including an arithmetic circuit for algebraically counting the zero scale output and ideal output and normalizing them by the least significant bit (LSB) value to obtain

the zero scale error coefficient and combining the full scale output and ideal output and normalizing them by the LSB to obtain the full scale error coefficient and applying those error coefficients to the input signal to the DAC.